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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,678	04/16/2004	Mikako Ujiie	XA-9730A	8657

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MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
PIZARRO CRESPO, MARCOS D	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,678	UJIIE ET AL.	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Attorney's Docket Number: XA-9730A

Filing Date: 4/16/2004

Claimed Priority Dates: 8/22/2002 (Divisional of 10/255,163)
9/18/2001 (JP 2001-283717)

Applicant(s): Ujiie, et al.

Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment filed on 9/1/2005.

Acknowledgment

1. The amendment filed on 9/1/2005 has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 31-36.

Specification

2. The disclosure is objected to because of the following informalities:

   - The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. Appropriate correction is required.

Drawings

4. The drawings received on 9/1/2005 are accepted.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claim 31, 32, and 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fontecha (US 6448507) in view of Baba (JP 7-45641).

8. Regarding claim 31, Fontecha shows (see, *e.g.*, figs. 1 and 2) most aspects of the instant invention including a method of manufacturing a semiconductor device comprising the steps of:

- ✓ Providing a wiring substrate **10** including:
  - A main surface
  - An insulating film **14** formed on the main surface
  - A plurality of electrodes **13** being exposed from the insulating film **14**

- ✓ Providing a semiconductor chip **11** having:
  - A main surface
  - A back surface
  - A plurality of semiconductor elements
  - A plurality of electrodes **16** formed on the main surface of the chip **11**
- ✓ Forming a groove **15** in the insulating film **14** so as to expose the main surface of the substrate **10** between the electrodes **13** and the chip **11**
- ✓ After forming the groove **15**, fixing the chip **11** to the insulating film **14** through a pasty adhesive **12**
- ✓ After fixing the chip, connecting one end of a plurality of conductive wires **17** to the plurality of electrodes **13** on the main surface of the wiring substrate **10**

wherein the fixing step is performed so as to allow a protruding portion of the pasty adhesive flowing out of the chip to stay in the groove so as not to reach the electrodes (see, *e.g.*, fig. 2)

Fontecha, however, fails to show the step of covering the chip, the main surface, and the conductive wires with a sealing resin, and that the pasty adhesive is formed on a peripheral surface of the chip as a slope surface by a raised portion of the adhesive.

Baba, in a similar method to Fontecha, shows a pasty adhesive **4** wherein a raised portion of the adhesive forms a sloped surface on the peripheral surface of the chip **2** (see, *e.g.*, fig. 1). He also performs a step of covering the chip, the main surface, and the conductive wires with a sealing resin to protect the semiconductor device (see, *e.g.*, par. 0010).

It would have been obvious at the time of the invention to one of ordinary skill in the art to have a raised portion of the adhesive forming a sloped surface on the peripheral surface of the chip, and to perform the step suggested by Baba of covering the chip, the main surface, and the conductive wires of Fontecha with a sealing resin to protect the semiconductor device.

9. Regarding claim 32, Fontecha shows that the conductive wires **17** are electrically connected between the electrodes **13** on the main surface of the substrate **10** and the electrodes **16** on the main surface of the chip **11** (see, *e.g.*, fig. 2).

10. Regarding claim 34, Baba/Fontecha shows that the step of fixing the chip comprises:

- ✓ Holding the chip with a bonding tool (see, *e.g.*, Baba/par.0003)
- ✓ Bringing the held chip into proximity with the insulating film (see, *e.g.*, Fontecha/fig. 2)
- ✓ Fixing the chip to the insulating film through the adhesive (see, *e.g.*, Fontecha/col.1/ll.25)

11. Regarding claim 35, Fontecha shows the chip **11** is located away from the groove **15** (see, *e.g.*, fig. 2).

12. Regarding claim 36, Fontecha shows (see, *e.g.*, figs. 1 and 2) most aspects of the instant invention including a method of manufacturing a semiconductor device comprising the steps of:

- ✓ Providing a wiring substrate **10** including:
  - A main surface

- An insulating film **14** formed on the main surface
- A plurality of electrodes **13** formed on the main surface
- A surface of the plurality of electrodes **13** being exposed from the insulating film **14**

✓ Providing a semiconductor chip **11** having:

- A main surface
- A back surface
- A plurality of semiconductor elements
- A plurality of electrodes **16** formed on the main surface

✓ Forming a groove **15** in the insulating film **14** so as to expose the main surface of the substrate **10** between the chip **11** and the electrodes **13** on the substrate **10**

✓ Fixing the chip **11** to the insulating film **14** through a pasty adhesive **12**

✓ After the fixing step, connecting one end of a plurality of wires **17** to the plurality of electrodes **13** on the main surface of the substrate **10**

Wherein:

✓ The fixing step is performed so as to allow a protruding portion of the pasty adhesive **12** flowing out of the chip **11** to stay in the groove **15** so as not to reach the electrodes **13** on the substrate **10**

✓ The semiconductor chip **11** is located away from the groove **15**

Fontecha, however, fails to show a step of covering the chip, the main surface of the substrate, and the wires with a sealing resin, and that the adhesive is formed on a peripheral surface of the chip as a slope surface by a raised portion of the adhesive.

Baba (see, *e.g.*, fig. 1), in a similar method to Fontecha, shows a pasty adhesive wherein a raised portion of the adhesive forms a sloped surface on the peripheral surface of the chip. He also performs a step of covering the chip, the main surface, and the conductive wires with sealing resin to protect the semiconductor device (see, *e.g.*, par.0010).

It would have been obvious at the time of the invention to one of ordinary skill in the art to have a raised portion of the adhesive forming a sloped surface on the peripheral surface of the chip, and to perform the step suggested by Baba of covering the chip, the main surface, and the conductive wires of Fontecha with a sealing resin to protect the semiconductor device.

13. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fontecha/Baba in view of Hasebe (US 2002/0084518).

14. Regarding claim 33, Fontecha/Baba shows most aspects of the instant invention (see, *e.g.*, paragraph 8 above), except for the groove extending to a region below the chip. Hasebe, however, teaches that doing so would allow to reduce the chip fixing area (bonding area), thereby reducing the size of the insulating film area (see, *e.g.*, par.0123). Hasabe's configuration also has improved heat transfer characteristics and stability (see, *e.g.*, par.0124).

It would have been obvious at the time of the invention to one of ordinary skill in the art to form Fontecha/Baba's groove extending to a region below the chip, as suggested by Hasabe, to reduce the size of the insulating film area where the chip is fixed and to obtain improved heat transfer characteristics and stability.

Response to Arguments

15. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

17. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

18. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814

Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(571) 273-8300**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 9:30 AM to 8:00 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

20. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 438/106-127	10/4/2005
Other Documentation:	
Electronic Database(s): EAST (USPAT, EPO, JPO)	10/4/2005

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